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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,375	07/25/2001	Hideyuki Furukawa	100353-00069	3493
4372	7590	06/29/2004	EXAMINER	
ARENT FOX KINTNER PLOTKIN & KAHN 1050 CONNECTICUT AVENUE, N.W. SUITE 400 WASHINGTON, DC 20036			ABRAHAM, ESAW T	
			ART UNIT	PAPER NUMBER
			2133	
DATE MAILED: 06/29/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/911,375	FURUKAWA, HIDEYUKI
	Examiner Esaw T Abraham	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on Amdt A filed on 04/01/04.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-4 and 7-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) 7-9 is/are allowed.
- 6) Claim(s) 1 and 4 is/are rejected.
- 7) Claim(s) 2 and 3 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 25 July 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

Final rejection

Response to the applicant's amendments

*****The amended claims (3, 7 and 8) are accepted by the examiner.

*****The 112, 2nd paragraph rejection made to reject claims 8 and 9 (in the first non-final office action) is withdrawn by the examiner.

Response to the applicant's argument

Applicants' argument with respect to original/amended claims 1 and 4 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection for claims 1 and 4 is made under 35 U.S.C. 103(a) as being unpatentable over Kishino (U.S. PN: 6,526,537)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

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4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims **1 and 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishino (U.S. PN: 6,526,537).

As per claims **1 and 4**, Kishino a storage capable of generating an ECC for data and adding the ECC to the data to thereby form a read/write unit includes a writing circuit for generating an ECC for N of write data received from a host, adding N equally divided ECC code parts to the N write data, respectively, to thereby form N write units, and writing the N write units to N continuous addresses of a semiconductor memory device, respectively. A reading circuit gathers the N equally divided ECC code parts contained in read data units read out of the N continuous addresses of the semiconductor memory device to thereby reconstruct the ECC, and corrects errors of the N read data units with the reconstructed ECC (see col. lines 3-16). Kishino further in figure 2 teaches an error detection (5) gathers the N equally divided ECC parts present in the data output from the read data registers 201-20n to thereby reconstruct a single ECC and further the error detection detects error bits out of the Nread data by using the reconstructed ECC and holds error bit information for a pre-selected period of time (see col. 4, lines 6-13). Furthermore, Kishino teaches that storing accurate data in a semiconductor memory device, it is a common practice to use an ECC system adding a preselected number of check bits necessary for an ECC to data bits, writing them in the memory device together, and detecting or correcting, based on the data bits and check bits, errors with an error detecting circuit at the time of data reading (see col. 1, lines 20-28). Kishino **does not explicitly teach** the exact terms such as “marking or identifying” a defect (an error) in a specific memory area or block. **However,**

such terms "identifying or marking" errors are known in the art to mean as detecting errors in a specific memory areas or blocks. **Therefore**, it would have been obvious at the time the invention was made to one of ordinary skill in the art to use such terms (marking or identifying errors) since detected errors are "error recognized, error marked or error identified" by a detection algorithm or mechanism. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because identifying or marking errors in a block are detecting faults and they are known terms in the art of memory detection systems.

Allowable subject matter

2. Claims **2 and 3** are objected to as being dependent upon a rejected base claim but would be allowable if rewritten independent from including all of the limitation of the base claim and any intervening claims.

The claimed invention comprises a method step of writing an ECC code includes the steps of suspending an ECC generation function to said semiconductor device and writing the ECC code from an exterior of said semiconductor memory device (as in claim 2) which the prior art do not teach or render obvious.

The claimed invention comprises a method of reading data from the defective block after the writing of ECC code, performing an ECC check on the read data and rejecting the semiconductor memory device as being defective if an ECC error is not detected (as in claim 3) which the prior art do not teach or render obvious.

3. Claim **7**, have been allowed.

Claims **8 and 9**, which are directly or indirectly dependents of claim 7 are also allowed over the prior art of record.

Conclusion

4. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (703) 305-7743. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham
Esaw Abraham

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Larry J. Lamarre
for

Albert DeCady
Primary Examiner